

Attorney Docket: 015685.P096

REMARKS

Claims 2, 4-17 and 19-31 are pending the above-referenced patent application. In this response, no claims have been canceled, added or amended.

The Examiner has rejected claims 2, 4-17 and 19-31 under 35 U.S.C. 103(a) as being unpatentable over Grisamore (U.S. Patent No. 6,535,901, hereinafter "Grisamore"); and has rejected claims 2, 4-17 and 19-31 under 35 U.S.C. 103(a) as being unpatentable over Costa (U.S. Patent No. 5,935,201, hereinafter "Costa"). These rejections are respectfully traversed. Reconsideration of the above-referenced patent application in view of the following remarks is respectfully requested.

It is well-established that to establish a prima facie case of obviousness, three basic criteria must be met. First, a suggestion or motivation must be shown, either in the cited documents themselves or in knowledge generally available to one of ordinary skill in the art, to modify a cited document or combine two or more cited documents. Second, a reasonable expectation of success in making this combination or modification must be shown. Third, it must be shown that the combination or modification, if proper, contains all of the elements of the claims under rejection. If any of these elements are not met, a successful prima facie case of obviousness has not been established.

It is respectfully submitted that neither Grisamore nor Costa meet all of the limitations of claim 2. As just an example, Grisamore does not recite "a Wallace-architecture of full-adders, half-adders and associated registers in the selected resources, the series of Boolean function generators to combine the input terms to produce intermediate summation results."

The Examiner already concedes that Grisamore is lacking at least one element of the rejected claims. According to the Examiner, "Grisamore does not teach registers in figures 5 and 9. However, Grisamore discloses that it is known in the art to use registers at optimal points in a multiplier to enable pipelined processing which provides a high through put multiply accumulate circuit." However, Grisamore clearly describes passing partial products from a partial product generator to a reduction tree module, and passing and subsequently retrieving carry terms from a memory device. [Col. 2:63-3:8.]. There is no contemplation throughout Grisamore to implement a method as recited in claim 2, including "a Wallace-architecture of full-adders, half-adders and associated registers".

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The Examiner states that it would have been obvious to a person of ordinary skill in the art to provide the Wallace-architecture of Grisamore with registers. However, one of ordinary skill in the art having Grisamore before him or her would be unable to produce the subject matter of the claims, and, therefore, Grisamore, by itself, would not render the rejected claims obvious. Further, Grisamore doesn't recognize the problem addressed by claim 2. As just an example, quoting from the detailed description, page 6, lines 12-17, "In accordance with another aspect of the invention, the hyperpipelined summing module architecture is extended to enable the input and processing of accumulator bits. By introducing the accumulator bits into register(s) of the hyperpipelined summing module, the summing module ... is extended to perform the function commonly associated with that of a conventional accumulator." Conversely, as conceded by the Examiner, Grisamore does not teach registers such as shown in figures 5 and 9.

It is respectfully submitted, therefore, that a prima facie case of obviousness under section 103 of the patent statute has not been made. It is noted that many other bases for traversing the rejection could be provided, but Assignee believes that the ground discussed above is sufficient. It is, therefore, respectfully submitted that the rejected claims are in a condition for allowance, and it is respectfully requested that the Examiner withdraw the rejection of claim 2.

Claims 4-16 depend from and include all limitations of claim 2. Therefore, it is respectfully submitted that these claims are in a condition for allowance on at least the same basis. Claims 17 and 19-31 contain limitations similar to claim 2, and are in a condition for allowance for at least the same reasons as claim 2.

Additionally, Costa does not meet all of the limitations of the rejected claims. As just an example, Costa does not recite "a Wallace-architecture of full-adders, half-adders and associated registers in the selected resources, the series of Boolean function generators to combine the input terms to produce intermediate summation results."

The Examiner already concedes that Costa is lacking at least one element of the rejected claims. According to the Examiner, "It is noted that Costa et al does not teach registers in the Wallace-architecture. However, since it is known in the art to use registers at optimal points in a multiplier to enable pipelined processing which provides a high through put multiply circuit (See col. 1, lines 33-41)."

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However, Costa describes a multiplier circuit to produce a final sum of partial products, and there is no contemplation throughout Costa to implement a method as recited in the rejected claims, including "a Wallace-architecture of full-adders, half-adders and associated registers".

The Examiner states that it would have been obvious to a person of ordinary skill in the art to provide the Wallace-architecture of Costa with registers. However, one of ordinary skill in the art having Costa before him or her would be unable to produce the subject matter of the claims, and, therefore, Costa, by itself, would not render the rejected claims obvious.

It is respectfully submitted, therefore, that a prima facie case of obviousness under section 103 of the patent statute has not been made. It is noted that many other bases for traversing the rejection could be provided, but Assignee believes that the ground discussed above is sufficient. It is, therefore, respectfully submitted that the rejected claims are in a condition for allowance, and it is respectfully requested that the Examiner withdraw the rejection of claim 2.

Claims 4-16 depend from and include all limitations of claim 2. Therefore, it is respectfully submitted that these claims are in a condition for allowance on at least the same basis. Claims 17 and 19-31 contain limitations similar to claim 2, and are in a condition for allowance for at least the same reasons as claim 2.

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CONCLUSION

In view of the foregoing, it is respectfully submitted that all of the claims pending in this patent application are in condition for allowance. If the Examiner has any questions, he is invited to contact the undersigned at (503) 640-6475. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

Please charge any shortages and credit any overcharges of any fees required for this submission to Deposit Account number 50-3130.

Respectfully submitted,



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